SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]   The present invention relates to a high-breakdown-voltage insulated gate semiconductor device using silicon carbide, and more particularly relates to a MOS field effect transistor (MOSFET) that provides a large-current switching device.

BACKGROUND ART

[0002]   Silicon carbide (SiC) is a semiconductor with a higher hardness and a wider band gap than silicon (Si) and applied to power devices, environmentally resistant devices, high-temperature operating devices, high-frequency devices, and other devices.

[0003]   For example, MOSFETs as disclosed in Patent Document 1 that will be described below are known as representative switching devices using SiC.   FIGS. **14(a)** and **14(b)** are diagrams showing typical vertical accumulation-mode MOSFETs using SiC. In a unit cell of a typical vertical MOSFET, a source electrode is arranged in the middle of the unit cell.   On the other hand, FIGS. **14(a)** and **14(b)** show the arrangement of electrodes with a gate electrode arranged in the middle.   That is, FIGS. **14(a)** and **14(b)** show a joint between two unit cells.   FIG. **14(a)** is a plan view showing some of electrodes of MOSFETs when seen from above, and FIG. **14(b)** is a cross-sectional view showing the MOSFETs taken along the line XI-XI shown in FIG. **14(a)**.

[0004]   As shown in FIGS. **14(a)** and **14(b)**, the known vertical accumulation-mode MOSFET comprises a semiconductor substrate **101** made of n⁺-type 4H-SiC, an n-type silicon carbide layer **102** formed on the semiconductor substrate **101** and made of n-type 4H-SiC, p-type well regions **103** formed in regions of the upper part of the n-type silicon carbide layer **102** located at both sides of the joint between the two unit cells and doped with, for example, aluminum, a channel layer **104** formed on a region of the n-type silicon carbide layer **102** interposed between the two p-type well regions **103** and the top surfaces

of the two p-type well regions and made of, for example, n-type 4H-SiC, source regions **105** formed in the upper parts of the p-type well regions **103** to come into contact with the lateral sides of the channel layer **104**, respectively, and doped with, for example, nitrogen, a gate insulating film **106** formed on the channel layer **104** and respective parts of the

5 source regions **105**, a gate electrode **107** formed on a part of the gate insulating film **106**, source electrodes **108** formed from on the top surface of the source regions **105** to on respective parts of the n-type silicon carbide layer **102** located to the outermost lateral sides of the source regions **105**, and a drain electrode **109** formed on the back surface of the semiconductor substrate **101**.

10 [0005] The source electrodes **108** each have a structure in which it also functions as base electrodes to which the p-type well regions **103** are electrically connected.

[0006] In order to turn the MOSFET ON, a positive voltage is applied to the drain electrode **109**, the source electrodes **108** are grounded, and a positive voltage is applied to the gate electrode **107**. In this way, switching operations of the MOSFET can be

15 achieved.

[0007] When the MOSFET is thus turned ON, electrons serving as carriers initially flow in the direction parallel to a substrate surface as shown in FIGS. **14(a)** and **14(b)**. Thereafter, the electrons flow in the direction perpendicular to the substrate surface as shown in FIG. **14(b)**. The arrows shown in FIGS. **14(a)** and **14(b)** show directions in

20 which electrons serving as carriers travel. Current flows in the opposite directions to these arrows. In this relation, the directions in which electrons travel in FIG. **14(a)** should be noted. The source electrodes **108** and the gate electrode **107** are arranged such that carriers travel in the direction perpendicular to a substrate miscut direction **A**. The "miscut direction" indicates the direction within a miscut surface inclined at an angle of

25 several degrees from the crystal plane and extending from a normal vector to the crystal plane toward a normal vector to the miscut surface. The reason why the electrodes are arranged as described above will be described hereinafter with reference to FIG. **15**. FIG.

15 is a perspective view schematically showing the top surface and cross sections of a silicon carbide substrate.

[0008]　　The silicon carbide substrate shown in FIG. 15 has a substrate surface miscut by a predetermined angle to the (0001) plane.　In FIG. 15, the substrate surface, i.e., the miscut surface is horizontally oriented.　Typically, when an element is formed using a silicon carbide substrate, a miscut substrate to the (0001) plane is used.　The reason for this is that if a layer is formed by epitaxial growth on a substrate surface miscut by a predetermined angle to the (0001) plane, the polytype can be easily controlled.　For example, the surface miscut by approximately 8 degrees from the 4H-SiC(0001) plane in the <11-20> direction (which herein means 11$\bar{2}$0) is formed as the miscut surface.

[0009]　　However, when a high-temperature process, such as epitaxial growth and heat treatment for dopant activation, is applied to a substrate having the miscut surface as the substrate surface, the step-bunching is developed at the substrate surface along the direction perpendicular to the miscut direction.　For example, when the miscut direction is the <11-20> direction, step bunches are formed to protrude along the <1-100> direction perpendicular to the <11-20> direction.　The step bunches have a height of approximately 50 through 100 nm, leading to anisotropy in electrical characteristics.　The electron mobility in the miscut direction (in the direction transverse to the step bunches) has conventionally differed, for example, by one or more orders of magnitude, from that in the direction perpendicular to the miscut direction (i.e., in the direction parallel to the step bunches).

[0010]　　In view of the above reason, in order to fabricate a semiconductor device capable of passing a large amount of current, electrodes has been required to be arranged such that current flows in the direction perpendicular to the miscut direction.　When currents flow through the channel layer 104 in a plurality of directions, electrodes need have been designed such that one of the plurality of directions in which the largest amount of current flows is matched with the direction perpendicular to the miscut direction (for

example, Patent Document 1).

Patent Document 1: Japanese Unexamined Patent Publication No. 2001-144288

Patent Document 2: PCT/JP98/01185

DISCLOSURE OF INVENTION

5 Problems that the Invention is to Solve

[0011]   As described above, the arrangement of elements has conventionally been determined based on the premise that the formation of step-bunching increases the electron mobility in the direction parallel to the step-bunching and decreases the electron mobility in the direction perpendicular thereto.   Even when no step-bunching is developed at the

10 surface of the substrate, crystal defects, such as stacking faults, exist in silicon carbide, and thus the electron mobility in the direction parallel to the miscut direction has sometimes become smaller than that in the direction perpendicular thereto.   However, in some cases, the anisotropy in the direction of current travel is reversed.   In this case, the electrical characteristics of elements have been deteriorated.

15 [0012]   It is an object of the present invention to provide a silicon carbide semiconductor device with more excellent electrical characteristics by taking a measure for solving the above problems.

Means of Solving the Problems

[0013]   A semiconductor device according to a first aspect of the present invention

20 comprises: a semiconductor substrate; a silicon carbide layer formed on the semiconductor substrate and having its top surface inclined at an angle of 10 degrees or less from a crystal plane in a miscut direction; a gate insulating film formed on the silicon carbide layer; a gate electrode formed on the gate insulating film; a source electrode formed on a part of the silicon carbide layer located to a side of the gate electrode; a drain electrode formed on

25 the back surface of the semiconductor substrate; and a source region formed in a region of the silicon carbide layer located at least under the source electrode, wherein the longest of the edges of the source region extends along the direction perpendicular to the miscut

direction in a plan view.

[0014] In this way, the source region is arranged to allow current to flow along the miscut direction, thereby improving electrical characteristics. Furthermore, the possibility that the current anisotropy is reversed is eliminated. The reason for the above is as follows. In the known art, step-bunching is developed in the direction perpendicular to the miscut direction of the silicon carbide layer during high-temperature heat treatment, and the electron mobility along the direction parallel to the step-bunching has been large. On the other hand, the semiconductor device of the present invention is formed through the step of heat treatment using a compound containing a group-V element. This reduces the interface state density at the interface between the gate insulating film and the silicon carbide layer, at which a channel layer is formed, and improves the electron mobility along the miscut direction even when the step-bunching is developed at the top surface of the silicon carbide layer. Therefore, the electron mobility along the miscut direction is likely to become higher than that in the direction perpendicular to the miscut direction.

[0015] The semiconductor device of the first aspect may further comprise: a well region of a second conductivity type formed in a part of the silicon carbide layer located on a lateral side of the source region and under the source region; and a base electrode electrically connected to the well region.

[0016] A direction extending along the direction perpendicular to the miscut direction may be a direction at an inclination of 5 degrees or less from the direction perpendicular to the miscut direction. Therefore, high electron mobility can be achieved.

[0017] A channel layer may be formed in a region of the silicon carbide layer located under the gate insulating film.

[0018] The channel region may have a multilayer structure including a first silicon carbide layer of at least one layer and a second silicon carbide layer of at least one layer having a higher first-conductivity-type dopant concentration and a smaller thickness than the first silicon carbide layer. In this case, higher electron mobility can be achieved.

[0019]   When the electron mobility through the silicon carbide layer is larger in the direction perpendicular to the crystal plane than in in-plane directions of the crystal plane, the present invention is effective.

[0020]   The silicon carbide layer may be 4H-SiC

[0021]   The top surface of the silicon carbide layer may be a plane inclined from the (0001) plane in the <11-20> direction.

[0022]   The top surface of the silicon carbide layer may be a plane inclined from the (0001) plane in the <1-100> direction.

[0023]   When the gate insulating film is formed by thermally oxidizing the upper part of the silicon carbide layer and subjecting the resultant upper part thereof to heat treatment in an atmosphere containing a compound inclusive of a group-V element, the interface state density can be reduced, resulting in the increased electron mobility in the miscut direction.

[0024]   When the compound inclusive of the group-V element is nitric oxide (N_xO_y(x, y = 1, 2, $\cdots$)), a large effect can be obtained.

[0025]   A maximum nitrogen concentration is preferably 1×10^{20} cm^{-3} through 1×10^{22} cm^{-3} both inclusive at the interface between the silicon carbide layer and the gate insulating film, i.e., at the interface between the channel layer and the gate insulating film.   In this case, the interface density within the potential range near each of band edges can be reduced enough.   Therefore, independently of whether or not the step-bunching is developed between the top surface of the silicon carbide layer and a gate oxide film, an excellent interface is formed therebetween.

[0026]   Even when the gate electrode is formed by subjecting the upper part of the silicon carbide layer to heat treatment in an atmosphere containing a compound inclusive of a group-V element, an excellent interface between the gate insulating film and the silicon carbide layer can be achieved.   In particular, the gate insulating film formed by heat treatment in an atmosphere containing the nitric oxide also works effectively to the

present invention.

[0027]   When the silicon carbide layer contains dopants of the first conductivity type and the semiconductor element of the first aspect comprises: the source electrode formed on a part of the silicon carbide layer located to a side of the gate electrode; the drain electrode formed on the back surface of the semiconductor substrate; and the source region of a first conductivity type formed in a region of the silicon carbide layer located at least under the source electrode and coming into contact with the channel layer; a well region of a second conductivity type formed in a part of the silicon carbide layer to cover one lateral side and the bottom of the source region; and a base electrode electrically connected to the well region, high electron mobility can be achieved in a vertical MOSFET.

[0028]   The source electrode may be formed using the same conductive film as the base electrode.

[0029]   The gate electrode may be formed to have a shape in which polygons are hollowed out in a plan view.   In this case, the longest of the edges of the hollowed polygons preferably extend along the direction perpendicular to the miscut direction.

[0030]   In this case, the source electrode may be formed in the shape of polygons in a plan view, and the gate electrode may be formed so as to be located apart from the source electrode and surround the lateral sides of the source electrode.

[0031]   The gate electrode may be formed in the shape of a polygon in a plan view. In this case, the longest of the edges of the polygon preferably extends along the direction perpendicular to the miscut direction.

[0032]   In this case, in a plan view, the source electrode may be formed to have a comb shape including a plurality of first rectangular parts arranged in stripes and a first connection part through which the respective one ends of the plurality of first rectangular parts are connected to one another, and the gate electrode may be formed to have a comb shape including a plurality of striped second rectangular parts arranged alternately with the plurality of first rectangular parts and a second connection part through which the

respective one ends of the plurality of second rectangular parts are connected to one another.

[0033]   Herein, a "polygon" and a "comb shape" include shapes having rounded corners or curved edges.   When the source region has, for example, an elliptical shape, "the longest of the edges of the source region extends along the direction perpendicular to the miscut direction" means that the major axis of the elliptical shape extends along the direction perpendicular to the miscut direction.

[0034]   A semiconductor device according to a second aspect of the present invention comprises: a semiconductor substrate; a silicon carbide layer formed on the semiconductor substrate and having its top surface inclined at an angle of 10 degrees or less from a crystal plane in a miscut direction; a gate insulating film formed on the silicon carbide layer; a gate electrode formed on the gate insulating film; a source electrode formed on a part of the silicon carbide layer located to one side of the gate electrode; a drain electrode formed on a part of the silicon carbide layer located to the other side of the gate electrode; and source/drain regions formed apart from each other in regions of the silicon carbide layer located at least under the source and gate electrodes, wherein the opposed two of the edges of the source/drain regions extend along the direction perpendicular to the miscut direction in a plan view.

[0035]   In this way, the source/drain regions are arranged to allow current to flow along the miscut direction, thereby improving electrical characteristics.   The reason for the above is as follows.   In the known art, step-bunching is developed in the direction perpendicular to the miscut direction of the silicon carbide layer during high-temperature heat treatment, and the electron mobility along the direction parallel to the step-bunching has been large.   On the other hand, the semiconductor element of the present invention is formed through the step of heat treatment using a compound containing a group-V element. This reduces the state density at the interface between the gate insulating film and the silicon carbide layer, at which a channel layer is formed, and improves the electron

mobility along the miscut direction even when the step-bunching is developed at the top surface of the silicon carbide layer. Therefore, the electron mobility along the miscut direction is likely to become higher than that in the direction perpendicular to the miscut direction.

[0036]   The semiconductor device of the second aspect may further comprise: a base region formed in the silicon carbide layer and containing dopants of a first conductivity type; and a base electrode electrically connected to the base region.

[0037]   The gate electrode may be formed in the shape of a polygon. In this case, the longest of the edges of the polygon preferably extends along the direction perpendicular to the miscut direction.

[0038]   A direction extending along the direction perpendicular to the miscut direction is a direction at an inclination of 5 degrees or less from the direction perpendicular to the miscut direction. Therefore, a high electron mobility can be achieved.

[0039]   A channel layer may be formed in a region of the silicon carbide layer located under the gate insulating film.

[0040]   The channel region may have a multilayer structure including a first silicon carbide layer of at least one layer and a second silicon carbide layer of at least one layer having a higher first-conductivity-type dopant concentration and a smaller thickness than the first silicon carbide layer. In this case, higher electron mobility can be achieved.

[0041]   When the electron mobility through the silicon carbide layer is larger in the direction perpendicular to the crystal plane than in in-plane directions of the crystal plane, the present invention is effective.

[0042]   The silicon carbide layer may be 4H-SiC.

[0043]   The top surface of the silicon carbide layer may be a plane inclined from the (0001) plane in the <11-20> direction.

[0044]   The top surface of the silicon carbide layer may be a plane inclined from the (0001) plane in the <1-100> direction.

[0045]   When the gate insulating film is formed by thermally oxidizing the upper part of the silicon carbide layer and subjecting the resultant upper part thereof to heat treatment in an atmosphere containing a compound inclusive of a group-V element, the interface state density can be reduced, resulting in the increased electron mobility in the miscut direction.

[0046]   When the compound inclusive of the group-V element is nitric oxide (N_xO_y(x, y = 1, 2, ···)), a large effect can be obtained.

[0047]   A maximum nitrogen concentration is preferably 1×10^{20} cm^{-3} through 1×10^{22} cm^{-3} both inclusive at the interface between the silicon carbide layer and the gate insulating film, i.e., at the interface between the channel layer and the gate insulating film.   In this case, the interface density within the potential range near each of band edges can be reduced enough.   Therefore, independently of whether or not the step-bunching is developed between the top surface of the silicon carbide layer and a gate oxide film, an excellent interface is formed therebetween.

[0048]   The source electrode may be formed using the same film as the base electrode.

Effect of the Invention

[0049]   According to the semiconductor device of the present invention, when the electron mobility reduced due to step-bunching and other unfavorable interface states is improved, this can provide more excellent electrical characteristics than those of a known structure of a semiconductor device.

BRIEF DESCRIPTION OF DRAWINGS

[0050]   [FIG. 1] FIGS. 1(a) and 1(b) are cross-sectional views showing a joint between two unit cells of typical vertical accumulation-mode MOSFETs using a silicon carbide layer in a first embodiment.

[FIG. 2] FIGS. 2(a) through 2(c) are cross-sectional views showing a procedure for forming a SiC-oxide layered structure.

[FIG. 3] FIG. 3 is a graph showing the nitrogen concentration profile where the nitrogen concentration in the thickness direction of a V-group element containing oxide layer 22 formed according to a production method of the first embodiment was measured by SIMS.

[FIG. 4] FIGS. 4(a) and 4(b) are graphs showing an interface state density calculated using a High-Low method based on data shown in FIG. 3.

[FIG. 5] FIG. 5 is a plan view showing the relationship between a direction in which carriers travel and the arrangement of elements in the semiconductor devices shown in FIG. 1.

[FIG. 6] FIG. 6(a) is a diagram showing, by vectors, a direction in which electrons travel and a length over which the electrons travel through a silicon carbide substrate having a (0001) plane as its top surface, and FIG. 6(b) is a diagram showing, by vectors, a direction in which electrons travel and a length over which the electrons travel through a silicon carbide substrate having, as its top surface, a plane inclined at an angle θ from the (0001) plane.

[FIG. 7] FIGS. 7(a) and 7(b) are diagrams showing the configuration of MOSFETs when gate and source electrodes are arranged in comb form.

[FIG. 8] FIGS. 8(a) and 8(b) are diagrams showing the configuration of MOSFETs when rectangular unit cells are arranged.

[FIG. 9] FIGS. 9(a) and 9(b) are diagrams showing the configuration of MOSFETs when hexagonal unit cells are arranged.

[FIG. 10] FIG. 10 is a cross-sectional view showing the configuration of vertical inversion-type MOSFETs.

[FIG. 11] FIGS. 11(a) and 11(b) are cross-sectional views showing typical lateral accumulation-mode MOSFETs using a silicon carbide layer according to a second embodiment.

[FIG. 12] FIG. 12 is a plan view showing the relationship between a direction in which carriers travel and the configuration of elements in the semiconductor device shown in FIG.

11(b).

[FIG. 13] FIG. **13** is a cross-sectional view showing the structure of lateral inversion-type MOSFETs.

[FIG. 14] FIGS. **14(a)** and **14(b)** are diagrams showing a joint between two unit cells of typical vertical accumulation-mode MOSFETs using SiC.

[FIG. 15] FIG. **15** is a perspective view schematically showing the top surface and cross section of a silicon carbide substrate.

Description of Numerals

[0051] 1A   interlayer insulating film

        1B   upper interconnect electrode

        7C   base electrode

        10   vertical accumulation-mode MOSFET

        11   semiconductor substrate

        12   n-type silicon carbide layer

        13   p-type well regions

        14   channel layer

        15   n-type source regions

        16   gate insulating film

        17   gate electrode

        18   source electrodes

        19   drain electrode

        20   SiC substrate

        21   oxide layer

        30   chamber

        31   vacuum pump

        60   vertical inversion-type MOSFET

        70   lateral accumulation-mode MOSFET

	71	semiconductor substrate
	72	p-type silicon carbide layer
	74	channel layer
	75d	drain region
5	75s	source region
	76	gate insulating film
	77	gate electrode
	78	source electrode
	79	drain electrode
10	90	lateral inversion-type MOSFET
	101	semiconductor substrate
	102	n-type silicon carbide layer
	103	p-type well regions
	104	channel layer
15	105	source regions
	106	gate insulating film
	107	gate electrode
	108	source electrodes
	109	drain electrode

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BEST MODE FOR CARRYING OUT THE INVENTION

[0052]   Embodiments of the present invention will be described hereinafter with reference to the drawings.

[0053]   (Embodiment 1)

25   FIGS. 1(a) and 1(b) are cross-sectional views showing a joint between two unit cells of typical vertical accumulation-mode MOSFETs using a silicon carbide layer in a first embodiment.   FIG. 1(a) is a plan view showing some of electrodes of the MOSFETs, and

FIG. 1(b) is a cross-sectional view taken along the line I-I in FIG. 1(a).

[0054]   As shown in FIGS. 1(a) and 1(b), a semiconductor device of this embodiment has an n^+-type 4H-SiC(0001) semiconductor substrate 11. The semiconductor substrate 11 has a surface miscut by approximately 8 degrees in the <11-20> direction, and its resistivity is approximately 0.02 Ωcm^2. An n-type 4H-SiC(0001) silicon carbide layer 12 is formed on the semiconductor substrate 11 to have a thickness of approximately 15 μm and doped with nitrogen at a concentration of 3 × 10^{15} cm^{-3}. The n-type silicon carbide layer 12 is formed on the semiconductor substrate 11 by epitaxial growth, and the influence of the semiconductor substrate 11 causes the top surface of the n-type silicon carbide layer 12 to have an off angle in the <11-20> direction.

[0055]   P-type well regions 13 are formed in regions of the upper part of the n-type silicon carbide layer 12 located to both lateral sides of the joint between the two unit cells in the following manner: the n-type silicon carbide layer 12 is doped with, for example, aluminum at a concentration of approximately 2 × 10^{18} cm^{-3} to a depth of approximately 0.8 μm, and then the aluminum-doped silicon carbide layer 12 is annealed at a high temperature of approximately 1700 degrees.

[0056]   A channel layer 14 of n-type 4H-SiC is formed to extend over a region of the top surface of the n-type silicon carbide layer 12 interposed between the two p-type well regions and the top surfaces of the two p-type well regions. In this embodiment, the channel layer 14 is a δ-doped layer obtained by alternately stacking undoped layers and doped layers containing n-type dopants at a concentration of approximately 5 × 10^{17} cm^{-3}. The channel layer 14 has a thickness of approximately 0.2 μm.

[0057]   Source regions 15 are formed in the upper parts of the p-type well regions 13 to come into contact with the lateral sides of the channel layer 14 in the following manner: the p-type well regions 13 are doped with, for example, nitrogen at a concentration of approximately 1 × 10^{19} cm^{-3} to a depth of approximately 0.3 μm, and then the nitrogen-doped p-type well regions 13 are annealed at a high temperature of approximately

1700 degrees.

[0058]   Basically, source regions **15** are formed by doping respective parts of the p-type well regions with n-type dopants, and a MOSFET **10** is a so-called double implantation MOSFET (DIMOSFET).   In FIG. **1**, the source regions are configured such that the channel layer is interposed therebetween.   A channel layer is deposited on the formed p-type well regions and furthermore n-type dopants are implanted into the n-type silicon carbide layer **12** from above the channel layer, thereby forming source regions. However, a semiconductor device may be achieved, for example, by forming p-type well regions and source regions and then a channel layer.

[0059]   A gate insulating film **16** with a thickness of approximately 60 nm is formed on the channel layer **14** and respective parts of the source regions **15** in the following manner: the respective upper parts of the source regions **15** and the channel layer **14** are thermally oxidized and then subjected to heat treatment under an atmosphere containing a V-group element.   A method for this heat treatment will be described below.

[0060]   A gate electrode **17** of aluminum is formed on the gate insulating film **16**.

[0061]   Source electrodes **18** of nickel are formed from on the source regions **15** to on respective parts of the n-type silicon carbide layer **12** located to the outermost lateral sides of the source regions **15** in the following manner: a nickel film is formed and then subjected to heat treatment at a temperature of approximately 1000 degrees.   This heat treatment allows the source electrodes **18** to make ohmic contact with the source regions **15**.   The source electrodes **18** function also as base electrodes electrically connected to the p-type well regions **13**.   In order to reduce the electrical resistance between the source electrodes **18** and the p-type well regions **13**, p^+-type ion implantation regions may be formed by implanting ions of aluminum into respective parts of the p-type well regions **13** located at their interfaces with the source electrodes **18** at a higher concentration than that in the respective other parts thereof.

[0062]   A drain electrode **19** of nickel is formed on the back surface of the

semiconductor substrate **11** in the following manner: a nickel film is formed and then subjected to heat treatment at a temperature of approximately 1000 degrees. This heat treatment allows the drain electrode **19** to make ohmic contact with the semiconductor substrate **11**.

5   [0063]   The gate electrode **17** is covered with an interlayer insulating film **1A**, and the interlayer insulating film **1A** and the source electrodes **18** are covered with an upper interconnect electrode **1B**.

[0064]   In order to turn the MOSFET **10** of this embodiment ON, a positive voltage is applied to the drain electrode **19**, the source electrodes **18** are grounded, and a positive

10   voltage is applied to the gate electrode **17**. In this way, switching operations of the MOSFET **10** can be achieved.

[0065]   When the MOSFET **10** is thus turned ON, electrons serving as carriers initially flow in the direction parallel to the substrate surface as shown in FIGS. **1(a)** and **1(b)**. In this relation, unlike the known art, in this embodiment, electrons flow in the direction

15   parallel to the offcut direction **A**. Thereafter, the electrons flow in the direction perpendicular to the substrate surface as shown in FIG. **1(b)**. The arrows shown in FIGS. **1(a)** and **1(b)** show directions in which electrons serving as carriers travel. Current flows in the opposite directions to these arrows.

[0066]   A method in which the gate insulating film **16** is formed and then subjected to

20   heat treatment will be described in detail with reference to the drawings. This method is disclosed in Japanese Patent Application Nos. 2003-350244 and 2004-271321 previously filed by the present applicant. The contents of the above-described applications are incorporated herein by reference.

[0067]   FIGS. **2(a)** through **2(c)** are cross-sectional views showing a procedure for

25   forming a SiC-oxide layered structure. Although in this embodiment nitrogen is used as a V-group element, any other V-group element, such as phosphorus (P) and arsenic (As), may be used.

[0068]   First, in the process step shown in FIG. 2(a), a SiC substrate 20 that is a 4H-SiC(0001) substrate is prepared.   The upper part of the SiC substrate 20 (a part of the SiC substrate 20 located above the broken line shown in FIG. 2(a)) is a 4H-SiC(0001) layer formed by epitaxial growth.   The principal surface of the SiC substrate 20 (an epitaxially grown SiC layer) is smoothed by MCP (mechano-chemical polishing) such that the difference in surface levels (maximum surface roughness Rmax) become 10 nm or less.   However, this smoothing process is not necessarily required.

[0069]   Next, in the process step shown in FIG. 2(b), the SiC substrate 20 is placed in a chamber 30 and heated under an oxidizing atmosphere, thereby forming an oxide layer 21 (primarily containing SiO_2) on the SiC substrate 20 to have an average thickness of approximately 60 nm.   In this case, an oxidizing temperature is 1000 °C or more, preferably 1050 through 1300 °C.   In order to produce an oxidizing atmosphere, a gas containing at least one of oxygen and water vapor need be allowed to flow through the chamber 30.   Thereafter, the oxide layer 21 is annealed in an inert gas atmosphere (Ar, N_2, He, Ne, or other gases) at a temperature of 1000 °C or more (for example, 1000 through 1150 °C).   The oxide layer 21 is densified in advance by this annealing process.

[0070]   Next, in the process step shown in FIG. 2(c), the SiC substrate 20 is moved into another chamber 30 having an exclusion device (not shown) and a vacuum pump 31 serving as a pressure reducer.   Then, a NO gas (or a gas containing a V-group element other than nitrogen (e.g., phosphorus (P)) is introduced into the chamber 30 at a flow rate of 500 (ml/min) while the inside pressure of the chamber 30 is reduced by the vacuum pump 31 to about 150 Torr (2.0×10^4 Pa), and the inside of the chamber 30 is heated to a temperature sufficient for nitrogen (or a V-group element other than nitrogen) to be diffused into the oxide layer 21 (e.g., about 1150°C).   Under the reduce pressure condition, the oxide layer 21 is exposed to the V-group element containing gas, such as nitrogen, whereby a V-group element, such as nitrogen, is diffused into the oxide layer 21. As a result, a denser V-group element containing oxide layer 22 having a large relative

dielectric constant is obtained. The exposure is performed for a time period which is sufficient for forming the dense V-group element containing oxide layer **22** and sufficient for obtaining improved characteristics of the V-group element containing oxide layer **22** (e.g., 1 hour). After the above-mentioned process steps, heat treatment is completed.

5   [0071] FIG. **3** is a graph showing the nitrogen concentration profile where the nitrogen concentration in the thickness direction of the V-group element containing oxide layer **22** formed according to the production method of this embodiment was measured by SIMS. More particularly, FIG. **3** shows the extracted concentration distribution of the peak portion (region near the SiO$_2$-SiC interface). The data shown in FIG. **3** was obtained by

10   quantitating nitrogen in the SiO$_2$-SiC interface with CsN[147]. As shown in FIG. **3**, the half-width of the peak portion was 3 nm, from which it is seen that nitrogen was introduced into a very narrow area with high concentration.

[0072] FIGS. **4(a)** and **4(b)** show the interface state density calculated using the High-Low method based on the data shown in FIG. **3**. In the graphs of FIGS. **4(a)** and

15   **4(b)**, the horizontal axis indicates the potential difference from valence band Ev (E-Ev (eV)), and the vertical axis indicates interface state density Dit (cm^{-2}eV^{-1}). In the case where the carrier in a MISFET is an electron, the interface state which functions as a trap is an interface state in the potential range near the conduction band edge (E-Ev = 2.95 eV to 3.05 eV). In the case where the carrier is a hole, the interface state which functions as a

20   hole trap is an interface state in the potential range near the valence band edge (E-Ev = 0.3 eV to 0.4 eV). However, as shown in FIGS. **4(a)** and **4(b)**, in this embodiment, the interface state density of 1×10^{12}cm^{-2}·eV^{-1} or lower was obtained in the potential range near each band edge. The average nitrogen concentration in the entire V-group element containing oxide layer **22** was 8.3×10^{19}cm^{-3}.

25   [0073] Thus, when a V-group element, such as nitrogen, is contained in the V-group element containing oxide layer **22**, the interface state density which functions as a carrier trap is decreased, and accordingly, the carrier mobility is improved.

[0074]   Especially because the maximum value of the nitrogen concentration in the lower part of the V-group element containing oxide layer **22** is equal to or higher than 1×10^{20} cm^{-3} and equal to or lower than 1×10^{22} cm^{-3}, the effect of improving the relative dielectric constant and the effect of decreasing the interface state density are significantly large.

[0075]   Next, the arrangement of the semiconductor devices of this embodiment will be described while being compared with that in the known art.

[0076]   In the known art, as shown in FIG. **14**, step-bunching is developed at the top surface of a substrate by the influence of high-temperature heat treatment for activating dopants ion-implanted into a layer.   Since the step-bunching is developed along the direction perpendicular to the miscut direction, the arrangement of electrodes or other elements has conventionally been determined such that more carriers flow in the direction perpendicular to the miscut direction.

[0077]   On the other hand, in this embodiment, elements are arranged such that more carriers flow substantially parallel to the miscut direction.   FIG. **5** is a plan view showing the relationship between the direction in which carriers travel and the arrangement of elements in the semiconductor devices shown in FIGS. **1**.   In FIG. **5**, the gate electrode **17**, the source electrodes **18** and some other elements are not shown, and only the n-type silicon carbide layer **12**, the p-type well regions **13** and the n-type source regions **15** are shown.   Although the channel layer **14** is not shown, the channel layer **14** is located on diagonally shaded regions of the p-type well regions **13**.   In a vertical MOSFET as shown in FIG. **5**, carriers flow from the source regions **15** toward the n-type silicon carbide layer **12**.   Elements are arranged such that the direction in which the carriers flow becomes substantially parallel to the miscut direction.

[0078]   -Principle on which the electron mobility increases in the miscut direction-

The known semiconductor device has the following anisotropy: the electron mobility is larger in the direction perpendicular to the miscut direction than in the direction parallel

thereto. On the other hand, in the semiconductor device of this embodiment, this anisotropy is reversed. The reason for this is that in this embodiment, heat treatment is performed using a gas containing nitrogen and oxygen, thereby reducing the interface state density at the interface between a silicon carbide layer and a gate insulating film and improving the electron mobility along the miscut direction. The reason why the electron mobility of the silicon carbide substrate is large in the cut-off direction will be examined hereinafter.

[0079] FIG. 6(a) is a diagram showing, by vectors, a direction in which electrons travel and a length over which the electrons travel through a silicon carbide substrate having a (0001) plane as its top surface. In FIG. 6(a), a vector parallel to the (0001) plane (designated crystal plane S) and the paper is designated as a vector **a**, a vector parallel to the (0001) plane but perpendicular to the paper is designated as a vector **b**, and a vector perpendicular to the (0001) plane is designated as a vector **c**.

[0080] In this case, the electron mobility of the silicon carbide layer whose top surface is the (0001) plane becomes larger in the direction perpendicular to the substrate surface than in in-plane directions of the substrate. More particularly, the vector **c** shown in FIG. 6(a) is larger than the vectors **a** and **b**. The vectors **a** and **b** have the same length.

[0081] Next, the case where the silicon carbide substrate is a miscut substrate will be examined. FIG. 6(b) is a diagram showing, by vectors, a direction in which electrons travel and a length over which the electrons travel through a silicon carbide substrate having, as its top surface, a plane inclined at an angle θ from the (0001) plane.

[0082] In FIG. 6(b), each of the vectors **a** and **c** are broken down into a vector extending along the miscut direction and a vector extending along the direction perpendicular to the miscut direction. The vectors corresponding to the vector **a** are designated as vectors **a1** and **a2**, and the vectors corresponding to the vector **c** are designated as **c1** and **c2**. In this case, when a vector indicating the electron mobility in the miscut direction is designated as a vector **d**, the vector **d** is expressed by the sum of the

vectors **a1** and **c1**.

[0083]   Since in this embodiment the vector **c** is larger than the vector **a**, the vector **d** becomes larger than the vector **a**.   On the other hand, since the vector **b** is perpendicular to the miscut direction, the electron mobility in the vector-**b** direction does not vary between when the top surface of the silicon carbide layer is the (0001) plane and when it is a miscut surface.   Since the vectors **a** and **b** have the same length, the vector **d** is obviously larger than the vector **b**.

[0084]   In view of the above, the electron mobility (vector **d**) in the miscut direction becomes larger than that (vector **b**) in the direction perpendicular to the miscut direction.

[0085]   As a matter of course, even when vectors indicating directions other than the vectors **b** and **d** are taken into account, it is obvious that the electron mobility in the miscut direction becomes largest within the miscut substrate surface.

[0086]   The electron mobility in the miscut direction is improved by a synergistic effect resulting from the combination of the above-mentioned effect of the vectors and the effect of reducing the interface state density at the interface between the silicon carbide layer and the gate insulating film by subjecting the silicon carbide layer to heat treatment using a gas containing nitrogen and oxygen.

[0087]   -Example of the arrangement of electrodes-

Shown in FIG. 1 is an example in which current is allowed to flow only along the direction parallel to the miscut direction A at the joint between the two unit cells. However, actually, current is allowed to flow along a plurality of directions in many vertical semiconductor devices.   In this case, elements are arranged such that one of the plurality of directions along which the largest amount of current flows becomes parallel to the miscut direction.   The structure of the vertical semiconductor device will be described hereinafter.

[0088]   (First arrangement example)

In vertical MOSFETs, a source electrode **18** and a gate electrode **17** may be arranged

in stripes (or in comb form). This case will be described with reference to FIGS. 7(a) and 7(b).

[0089]   FIGS. 7(a) and 7(b) are diagrams showing the configuration of MOSFETs when the gate and source electrodes are arranged in comb form. FIG. 7(a) shows the configuration of a gate electrode 17 and a source electrode 18, and FIG. 7(b) shows the configuration of an n-type silicon carbide layer 12, p-type well regions 13 and n-type source regions 15. As shown in FIG. 7(a), a plurality of rectangular parts of the source electrode 17 are arranged in stripes. Respective one ends of the plurality of rectangular parts of the source electrode 17 are electrically connected to one another by making contact with a connection part of the source electrode 17 extending perpendicularly to the direction along which the rectangular parts thereof extend. A plurality of rectangular parts of the gate electrode 18 are arranged in stripes alternately with the rectangular parts of the source electrode 17. Respective one ends of the plurality of rectangular parts of the gate electrode 18 are electrically connected to one another by making contact with a connection part of the gate electrode 18 extending perpendicularly to the direction along which the rectangular parts thereof extend. A channel region is arranged in diagonally shaded regions shown in FIG. 7(b). In this case, the directions in which carriers travel are given two directions, i.e., the directions A and B. The channel region primarily extends along the direction perpendicular to the direction A. In view of the above, elements are arranged such that the width W1 of the channel region through which current is allowed to flow along the direction A is equal to or larger than the other width W2 of the channel region. The longest edges of each n-type source region 15 are also oriented perpendicularly to the miscut direction A.

[0090]   (Second arrangement example)

A vertical MOSFET is arranged for each of polygonal unit cells, in each of which the lateral sides of a source electrode may be surrounded by a gate electrode. This case will be described with reference to FIGS. 8(a) and 8(b).

[0091]   FIGS. 8(a) and 8(b) are diagrams showing the configuration of vertical MOSFETs when rectangular unit cells are arranged.   FIG. 8(a) shows the configuration of a gate electrode 17 and a source electrode 18, and FIG. 8(b) shows the configuration of an n-type silicon carbide layer 12, p-type well regions 13 and n-type source regions 15.

5   Channel regions are arranged in diagonally shaded regions shown in FIG. 8(b).

[0092]   In this case, the directions in which carriers travel are given two directions, i.e., the directions A and B.   When the longitudinal direction of each unit cell is set perpendicularly to the direction A, parts of each channel region extending along the direction perpendicular to the direction A become longer than parts of the channel region

10   extending along the direction parallel thereto.   In view of the above, as shown in FIG. 8(b), elements are arranged such that the width W1 of the channel region through which current is allowed to flow along the direction A is equal to or larger than the other width W2 thereof.   The longest edges of each n-type source region 15 are also oriented perpendicularly to the miscut direction A.

15   [0093]   Although in this example a case where the unit cell is rectangular was described, the unit cell may have a polygonal shape, such as a parallelogram or a rhombus. FIGS. 9(a) and 9(b) are diagrams showing the configuration of vertical MOSFETs when hexagonal unit cells are arranged.   FIG. 9(a) shows the configuration of a gate electrode 17 and source electrodes 18, and FIG. 9(b) shows the configuration of a n-type silicon

20   carbide layer 12, p-type well regions 13 and n-type source regions 15.   Channel regions are arranged in diagonally shaded regions shown in FIG. 9(b).

[0094]   In this case, there are primarily three directions in which carriers travel, i.e., directions A, C and D.   When the longest two of the edges of each hexagonal unit cell are arranged perpendicularly to the direction A, parts of the channel regions extending along

25   the direction perpendicular to the direction A become longer than parts thereof extending along the direction perpendicular to the directions C and D.   In view of the above, as shown in FIG. 9(b), elements are arranged such that the width W1 of each of parts of the

channel regions through which current flows along the direction **A** becomes equal to or larger than the width **W2** of each of the other parts of the channel regions through which current flows along the other directions. The longest edges of each n-type source region **15** are also oriented perpendicularly to the miscut direction **A**.

[0095] The method described in this embodiment can be applied not only to the case where the δ-doped layer is used as the channel layer but also to the case where the channel layer is a usual n-type dopant layer.

[0096] Furthermore, the method described in this embodiment can also be applied to a vertical inversion-type MOSFET **60**. FIG. **10** is a cross-sectional view showing the configuration of vertical inversion-type MOSFETs. Unlike FIG. **1**, in FIG. **10**, the channel layer (shown in FIG. **1**) is not formed. Since the other structure of each MOSFET is the same as that in FIG. **1**, a description thereof is not given.

[0097] (Embodiment 2)

FIGS. **11(a)** and **11(b)** are cross-sectional views showing typical lateral accumulation-mode MOSFETs using a silicon carbide layer according to a second embodiment. FIG. **11(a)** is a plan view showing some of electrodes of the MOSFETs when seen from above, and FIG. **11(b)** is a cross-sectional view taken along the line VII-VII in FIG. **11(a)**.

[0098] As shown in FIGS. **11(a)** and **11(b)**, a semiconductor device of this embodiment has a semi-insulating 4H-SiC(0001) semiconductor substrate **71**. The semiconductor substrate **71** has a surface miscut by approximately 8 degrees in the <11-20> direction. A 4H-SiC(0001) p-type silicon carbide layer **72** is formed on the semiconductor substrate **71** to have a thickness of approximately 5 μm and doped with aluminum at a concentration of 5×10^{15} cm^{-3}.

[0099] An n-type channel layer **74** is formed in the middle region of the upper part of the p-type silicon carbide layer **72**. In this embodiment, the channel layer **74** is a δ-doped layer obtained by alternately stacking undoped layers and doped layers containing n-type

dopants at a concentration of approximately 5×10^{17} cm^{-3}. The channel layer **74** has a thickness of approximately 0.2 µm.

[0100]   A source region **75s** and a drain region **75d** are formed in regions of the p-type silicon carbide layer **72** located to both sides of the channel layer **74** in the following manner: for example, the p-type silicon carbide layer **72** is doped with nitrogen at a concentration of approximately 1×10^{19} cm^{-3} to a depth of about 0.3 µm, and then the nitrogen-doped p-type silicon carbide layer **72** is annealed at a high temperature of about 1700 degrees.

[0101]   In principle, the source region **75s** and the drain region **75d** are formed by doping parts of a p-type well region with n-type dopants.   A MOSFET **70** is a so-called double implantation MOSFET (DIMOSFET).

[0102]   In FIGS. **11(a)** and **11(b)**, the channel layer is sandwiched between the source and drain regions.   A p-type well region is formed, then a channel layer is deposited thereon, and furthermore the p-type well region is doped with n-type dopants from above the channel layer, thereby forming source and drain regions.   A semiconductor device may be achieved by forming a p-type well region and source and drain regions and then a channel layer.

[0103]   A gate insulating film **76** with a thickness of about 60 nm is formed over the channel layer **74** and respective one lateral end parts of the source region **75s** and the drain region **75d** in the following manner: the respective upper parts of the channel layer **74**, the source region **75s** and the drain region **75d** are thermally oxidized, and then the thermally oxidized upper parts thereof are subjected to heat treatment in an atmosphere containing a V-group element.

[0104]   A gate electrode **77** of aluminum is formed on part of the gate insulating film **76**.

[0105]   A source electrode **78** of nickel is formed on part of the source region **75s**, and a drain electrode **79** of nickel is formed on part of the drain region **75d**.   A source

electrode 78 and a drain electrode 79 are formed in the following manner: a nickel film is formed, and then the nickel film is subjected to heat treatment at a temperature of about 1000 degrees. This heat treatment allows the source region 75s and the drain region 75d to make ohmic contact with the source electrode 78 and the drain electrode 79,

5 respectively.

[0106] A base electrode 7C is formed on a region of the p-type silicon carbide layer 72 located to the outer lateral side of the source region 75s to electrically connect the p-type silicon carbide layer 72 to the outside. In order to reduce the electrical resistance between the base electrode 7C and the p-type silicon carbide layer 72, a p^+-type ion implantation

10 region may be formed by implanting ions of aluminum into a part of the p-type silicon carbide layer 72 located at the interface therebetween at a higher concentration than that in the other part thereof. Furthermore, the source electrode 78 and the base electrode 7C may be electrically joined with each other or made of the same conductive film.

[0107] In order to turn the MOSFET 70 of this embodiment ON, a positive voltage is

15 applied to the drain electrode 79, the source electrode 78 and the base electrode 7C are grounded, and a positive voltage is applied to the gate electrode 77. In this way, switching operations of the MOSFET 70 can be achieved.

[0108] When the MOSFET 70 is thus turned ON, electrons serving as carriers flow from the source region 75s toward the drain region 75d in the direction parallel to the

20 substrate surface as shown in FIGS. 11(a) and 11(b). In this relation, unlike the known art, in this embodiment, electrons flow in the direction parallel to the miscut direction A. The configuration of semiconductor devices of this embodiment will be described below with reference to FIG. 12. FIG. 12 is a plan view showing the relationship between a direction in which carriers travel and the configuration of elements in the semiconductor

25 devices shown in FIG. 11(b). In FIG. 12, the gate electrode 77, the source electrode 78, the drain electrode 79, and other elements are not shown, and only the p-type silicon carbide layer 72, the n-type source region 75s and the n-type drain region 75d are shown.

Although the channel layer 74 is not shown, it is located on a diagonally shaded region of the p-type silicon carbide layer 72. As shown in FIG. 12, in a lateral MOSFET, carriers travel in the direction from the source region 75s toward the drain region 75d. Elements are arranged such that this direction becomes substantially parallel to the miscut direction

5   A.

[0109]   In many lateral elements, current flowing therethrough is unidirectional. In some lateral elements, however, current flows in two or more directions. In this case, elements are arranged such that the dominating current flows in the direction parallel to the miscut direction A of the substrate. More particularly, elements are arranged such that

10   one W1 of the widths of the channel region across which current flows through the channel region along the direction A becomes equal to or larger than the other width or widths thereof. In other words, elements are arranged such that the respective opposed edges of the source region 75s and the drain region 75d (the respective edges thereof coming into contact with the channel layer 74) become perpendicular to the miscut direction A.

15   [0110]   The method described in this embodiment can be applied to not only the case where a δ-doped layer is used as the channel layer but also the case where the channel layer is a usual n-type dopant layer.

[0111]   Furthermore, the method described in this embodiment can be applied to a lateral inversion-type MOSFET. FIG. 13 is a cross-sectional view showing the

20   configuration of lateral inversion-type MOSFETs. In FIG. 13, unlike FIG. 11(b), a channel layer 74 (shown in FIG. 11(b)) is not formed. The other structure of each MOSFET is the same as that in FIG. 11(b), and thus a description thereof is not given.

[0112]   (Other embodiments)

In the previously-described embodiments, a substrate having a surface miscut by

25   approximately 8 degrees from 4H-SiC is used as a semiconductor substrate. However, in the present invention, any other substrate may be used as long as it has a surface inclined at an angle of 10 degrees or less from the designated crystal plane S in a predetermined

direction A.

[0113] In the present invention, for example, a silicon carbide layer heteroepitaxially grown on a miscut Si substrate may be used.

[0114] In the previously-described embodiments, a 4H-SiC silicon carbide layer is used. However, in the present invention, a silicon carbide layer of any other polytype crystal structure may be used as long as the polytype crystal structure has characteristics that make the electron mobility larger in the direction perpendicular to the crystal plane than in in-plane directions of the crystal plane.

[0115] If a miscut substrate, in spite of a polytype crystal structure having characteristics that make the electron mobility smaller in the direction perpendicular to the crystal plane than in in-plane directions of the crystal plane has a possibility that the electron mobility becomes larger in the miscut direction than in the direction perpendicular to the miscut direction, this miscut substrate may be used.

[0116] In the previously-described embodiments, a semiconductor substrate miscut in the <11-20> direction is used as a 4H-SiC(0001) substrate. However, in the present invention, a substrate miscut in the <11-20> direction or the <1-100> direction may be used as a semiconductor substrate. In this case, when a silicon carbide layer is epitaxially grown on the semiconductor substrate, the top surface of the silicon carbide layer is a plane miscut from the (0001) plane in the <11-20> direction or the <1-100> direction. However, as long as a desired plane comes to the top surface of the silicon carbide layer, the plane orientation and miscut direction of the semiconductor substrate located below the silicon carbide layer are not particularly restrictive. In other words, as long as the longest of the edges of the source region are configured to extend along the direction perpendicular to the miscut direction, the miscut direction may be any other direction than the previously-mentioned miscut direction.

[0117] The (0001) plane of silicon carbide typically represents a silicon plane. However, a carbon plane represented as a (000-1) plane may be used instead of the (0001)

plane.

[0118]   Such a state that the electron mobility through silicon carbide becomes larger in the miscut direction than in the other directions can be achieved when the interface state density at the interface between a channel region of a MOSFET and a gate insulating film thereof is 5×10^{12} cm^{-2}·eV^{-1} or less at an energy level that is 0.1 eV smaller than the energy level of the conduction band of silicon carbide.   It is preferable that the interface state density at the above-described interface is 1×10^{12} cm^{-2}·eV^{-1} or less.   On the contrary, when the interface state density is larger than 5×10^{12} cm^{-2}·eV^{-1}, the influence of step-bunching produced at the above-described interface makes the electron mobility smaller in the miscut direction (perpendicular to the step-bunching) than in the direction parallel to the step-bunching like known silicon carbide semiconductor devices.

[0119]   In the previously-described embodiments, in order to reduce the interface state density at the interface between the silicon carbide layer and the gate insulating film, heat treatment is performed in an atmosphere containing nitric oxide (NO) after the formation of the gate insulating film.   However, in the present invention, the same effect can be obtained by heat treatment in an atmosphere containing a group-V element.   If the interface state density can be reduced, heat treatment may be performed in any other atmosphere or any other processing method may be used.

[0120]   In the previously-described embodiments, nickel or aluminum is used as an electrode material.   However, in the present invention, the electrode material is not limited to these materials, and an electrode may have a multilayer structure.

[0121]   In the fabrication method for a silicon carbide semiconductor device of the present invention, any method except for the fabrication method described in the embodiments may be used.   Unless otherwise designated, conditions and gas types are not limited to those for the process described herein.   The silicon carbide semiconductor device may be fabricated on any other conditions.

[0122]   As a matter of course, the silicon carbide semiconductor device of the present

invention can have various modifications as long as the modifications have the same principal structure within the scope of the invention.

INDUSTRIAL APPLICABILITY

5   The semiconductor device of the present invention has a high industrial applicability in that the electron mobility through a silicon carbide layer, which has been reduced due to step-bunching or the other unfavorable interface state, is improved, thereby achieving excellent electrical characteristics.